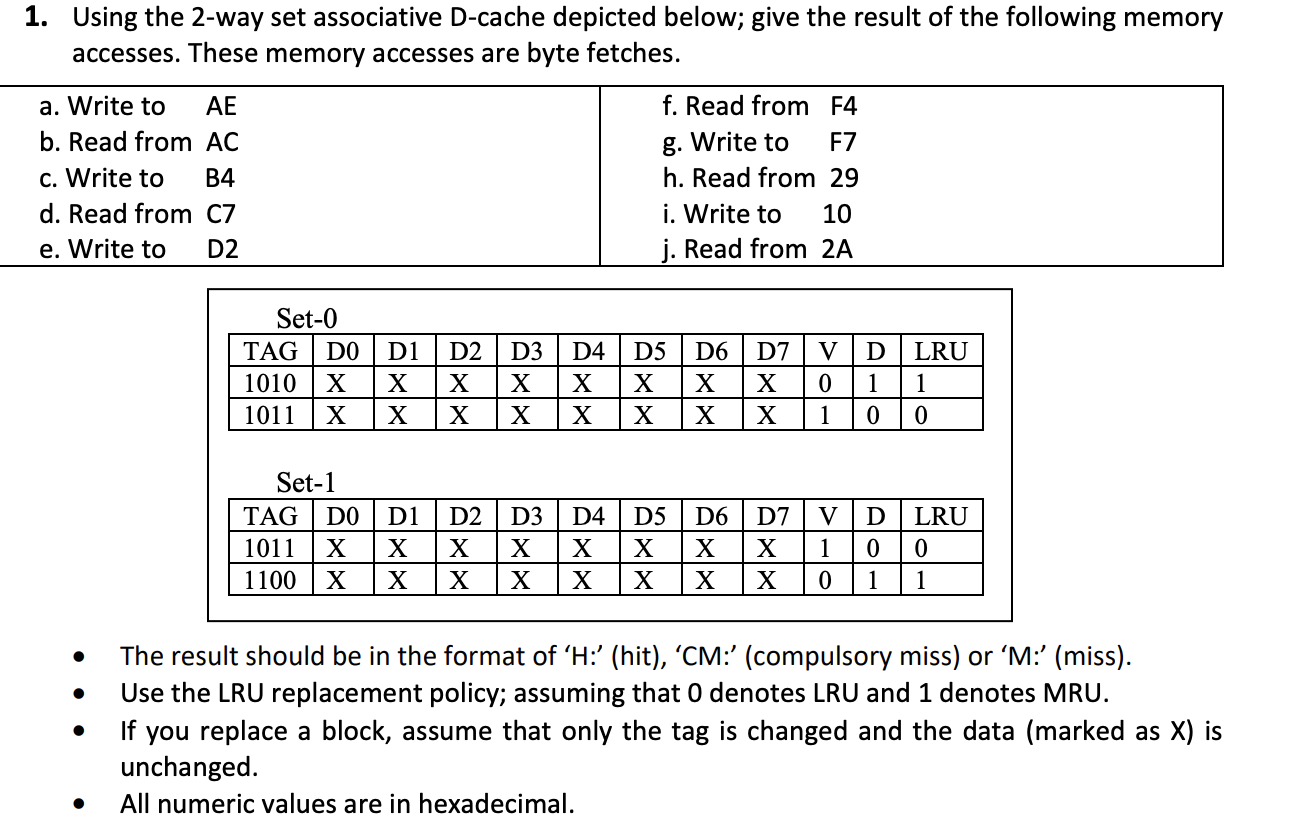
ASSIGNMENT 4



From the cache, tag bits = 4 bits.

we have 2 sets, so index bits = log 2 =1 bits.

so the bits are configured as:

|  |  |  |
| --- | --- | --- |
| Tag(4 bits) | Index(1 bits) | Block Offset(3 bits) |

A) AE

1010 1110

tag = 1010 in set 1. This is a MISS. So the cache would be charged as follows:

SET 0:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1010 | X | X | X | X | X | X | X | X | 0 | 1 | 1 |
| 1011 | X | X | X | X | X | X | X | X | 1 | 0 | 0 |

SET 1:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1011 | X | X | X | X | X | X | X | X | 1 | 0 | 1 |
| 1010 | X | X | X | X | X | X | X | X | 1 | 1 | 0 |

B) AC = 1010 1100 - HIT.

C)B4= 1011 0111 = TAG=1011, SET#=0. HIT.

SET 0:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1010 | X | X | X | X | X | X | X | X | 0 | 1 | 1 |
| 1011 | X | X | X | X | X | X | X | X | 1 | 0 | 0 |

SET 1:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1011 | X | X | X | X | X | X | X | X | 1 | 0 | 1 |
| 1010 | X | X | X | X | X | X | X | X | 1 | 1 | 0 |

D) C7 = 1100 0111 = TAG=1100, SET#=0. THIS IS A MISS.

SET 0:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1010 | X | X | X | X | X | X | X | X | 0 | 1 | 1 |
| 1100 | X | X | X | X | X | X | X | X | 1 | 0 | 0 |

SET 1:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1011 | X | X | X | X | X | X | X | X | 1 | 0 | 1 |
| 1010 | X | X | X | X | X | X | X | X | 1 | 1 | 0 |

E) D2 = 1101 0010 = TAG=1101, SET#=0. THIS IS A MISS.

SET 0:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1101 | X | X | X | X | X | X | X | X | 1 | 1 | 1 |
| 1100 | X | X | X | X | X | X | X | X | 1 | 0 | 0 |

SET 1:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1011 | X | X | X | X | X | X | X | X | 1 | 0 | 1 |
| 1010 | X | X | X | X | X | X | X | X | 1 | 1 | 0 |

F) F4 = 1111 0100

TAG=1111, SET#=0. THIS IS A MISS.

SET 0:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1111 | X | X | X | X | X | X | X | X | 1 | 1 | 0 |
| 1100 | X | X | X | X | X | X | X | X | 1 | 0 | 1 |

SET 1:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1011 | X | X | X | X | X | X | X | X | 1 | 0 | 1 |
| 1010 | X | X | X | X | X | X | X | X | 1 | 1 | 0 |

G) F7: 1111 0111 = TAG=1111, SET#=0. THIS A HIT. NO CHANGES IN CACHE.

H) 29 = 0010 1001 = TAG=0010 , SET#=1. THIS IS A MISS.

SET 0:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1111 | X | X | X | X | X | X | X | X | 1 | 1 | 0 |
| 1100 | X | X | X | X | X | X | X | X | 1 | 0 | 1 |

SET 1:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 0010 | X | X | X | X | X | X | X | X | 1 | 0 | 0 |
| 1010 | X | X | X | X | X | X | X | X | 1 | 1 | 1 |

I) 10 = 0001 0000 = TAG=0001, SET#=0. THIS A MISS.

SET 0:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1111 | X | X | X | X | X | X | X | X | 1 | 1 | 1 |
| 0001 | X | X | X | X | X | X | X | X | 1 | 0 | 0 |

SET 1:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 0010 | X | X | X | X | X | X | X | X | 1 | 0 | 0 |
| 1010 | X | X | X | X | X | X | X | X | 1 | 1 | 1 |

J) 2A = 0010 1010 = TAG= 0010, SET#=1. THIS IS A HIT.

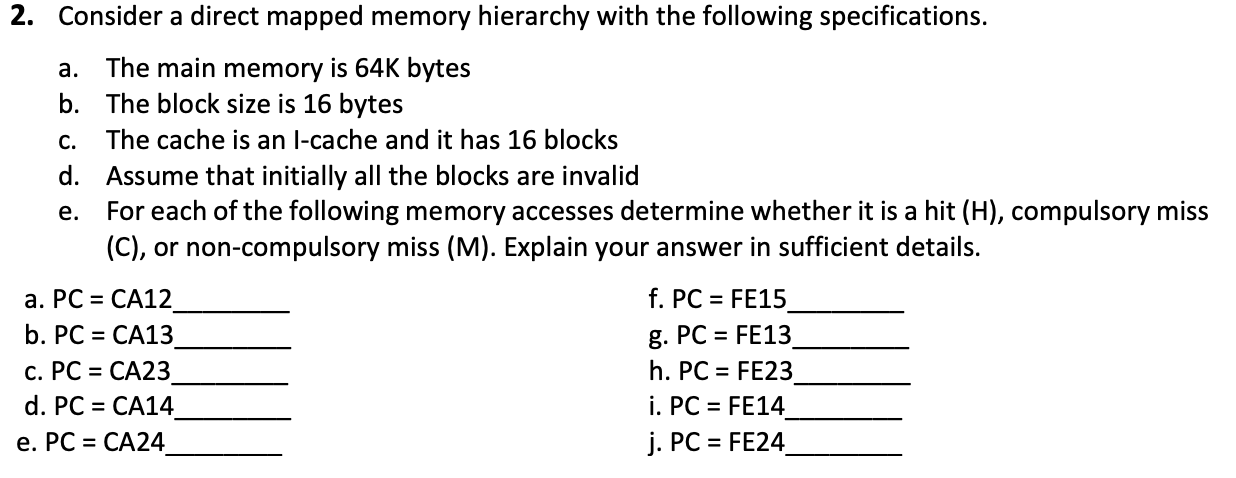
FINAL CACHE CONTENT IS:

SET 0:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 1111 | X | X | X | X | X | X | X | X | 1 | 1 | 1 |
| 0001 | X | X | X | X | X | X | X | X | 1 | 0 | 0 |

SET 1:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| TAG | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | V | D | LRU |
| 0010 | X | X | X | X | X | X | X | X | 1 | 0 | 0 |
| 1010 | X | X | X | X | X | X | X | X | 1 | 1 | 1 |



Memory size: 64KB = 2^16B  
Block size: 16B = 2^4B  
No.of cache blocks = 16  
Cache size: No.of blocksXBlock size = 16X16B=2^8B

The main meory can be represented with 16 bits.  
The block offset/size can be represented with 4 bits.  
The cache line can be represented with 4 bits.  
Tag = 16-(4+4)=16-8=8.

So, the main memory format is like below.

|  |  |  |
| --- | --- | --- |
| Tag(8) | Line(4) | Offset(4) |

* The the first 8 bits represents tag .
* Next 4 bits represents line number
* Next 4 bits represents offset
* The first 12 bits represents memory block address.

Note: when a memory block is loaded into one cache block total 16 Bytes are loaded into the cache.

i.e each block offset from 0000 to 1111

a. PC:CA12

|  |  |  |
| --- | --- | --- |
| 11001010 | 0001 | 0010 |

Memory block number :: 110010100001 -- 3233

Cache block number is 0001 -- 1.

It is compulsury miss, since it is the first time miss.

b. PC:CA13

|  |  |  |
| --- | --- | --- |
| 11001010 | 0001 | 0011 |

Memory block number :: 11001010001 -- 3233

Cahe block number is 0001 -- 1 .

It is hit since already memory block number 3233 is loaded in cache block number 1.

c. PC:CA23

|  |  |  |
| --- | --- | --- |
| 11001010 | 0010 | 0011 |

Memory block number :: 11001010010 -- 3234

Cahe block number is :: 0010 -- 2 .

It is compulsury miss, since it is the first time miss.

d. PC:CA14

|  |  |  |
| --- | --- | --- |
| 11001010 | 0001 | 0100 |

Memory block number :: 11001010001 -- 3233

Cahe block number is 0001 -- 1 .

It is hit since already memory block number 3233 is loaded in cache block number 1.

e. PC:CA24

|  |  |  |
| --- | --- | --- |
| 11001010 | 0010 | 00100 |

Memory block number :: 11001010010 -- 3234

Cahe block number is 0010 -- 2 .

It is hit since already memory block number 3234 is loaded in cache block number 2.

f. PC:FE15

|  |  |  |
| --- | --- | --- |
| 11111110 | 0001 | 0101 |

Memory block number :: 111111100001 -- 4065

Cahe block number is 0001 -- 1 .

It is compulsury miss, since it is the first time miss.

g. PC:FE13

|  |  |  |
| --- | --- | --- |
| 11111110 | 0001 | 0011 |

Memory block number :: 111111100001 -- 4065

Cahe block number is 0001 -- 1 .

It is hit since already memory block number 4065 is loaded in cache block number 1.

h. PC:FE23

|  |  |  |
| --- | --- | --- |
| 11111110 | 0010 | 0011 |

Memory block number :: 111111100010 -- 4066

Cahe block number is 0010 -- 2 .

It is compulsury miss, since it is the first time miss.

i. PC:FE14

|  |  |  |
| --- | --- | --- |
| 11111110 | 0001 | 0100 |

Memory block number :: 111111100001 -- 4065

Cahe block number is 0001 -- 1 .

It is hit since already memory block number 4065 is loaded in cache block number 1.

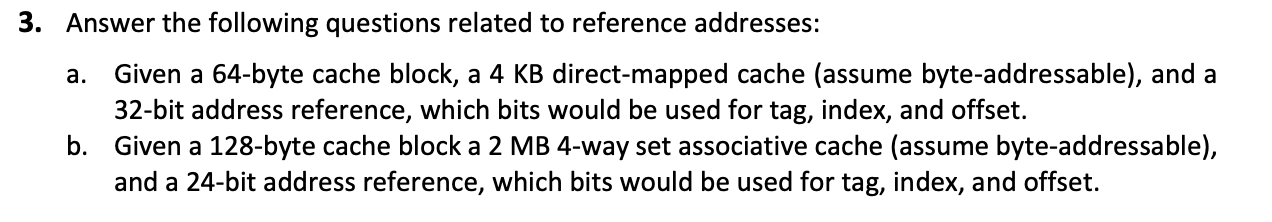
j. PC:FE24

|  |  |  |
| --- | --- | --- |
| 11111110 | 0010 | 0100 |

Memory block number :: 111111100010 -- 4066

Cahe block number is 0010 -- 2 .

It is hit since already memory block number 4066 is loaded in cache block number 2.



1. 64 byte cache block = 26 byte

6 bit for offset

Cache size = 4 kb = 212 byte

No. of cache block = 212/26  = 26

6 bit for index

Tag bit = 32 – 6 -6 = 20 bit

Tag = 20, index = 6, offset = 6

1. 128 byte cache block = 27 byte

7 but for offset

Cache size = 2MB = 221 byte

No. of set = 221/ 27 \* 4 = 221 / 211 = 210

10 bit

Tag bit = 24 – 10 – 7 = 7

Tag = 7

Index = 10

Offset = 7